| Ousmane Toure & Jianning Chen  EECE2160 | Embedded Design: Enabling Robotics  Lab Assignment 1 |
| --- | --- |

Lab Assignment 1

Introduction to Hardware

Ousmane Toure & Jianning Chen

[Toure.o@northeastern.edu](mailto:Toure.o@northeastern.edu)

[chen.jiann@northeastern.edu](mailto:chen.jiann@northeastern.edu)

Submit date: 5/12/2022

Due Date: 5/13/2022

**1.0 Schematics**

There was an error in the prelab truth table, which caused an incorrect output for c. This is the edited and revised Truth tables with minterm solutions in SOP.

|  | **INPUTS** | |  | **Character** |  |  |  | **OOUTPUTS** | |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D3** | **D2** | **D1** | **D0** | **#** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 2 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 3 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 4 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 5 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 6 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 7 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 9 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | A | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | b | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | c | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | d | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | E | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | F | 1 | 0 | 0 | 0 | 1 | 1 | 1 |

| Inverted Table | **INPUTS** | |  | **Character** |  |  |  | **OOUTPUTS** | |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D3** | **D2** | **D1** | **D0** | **#** | **a** | **b** | **c** | **d** | **e** | **f** | **g** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 3 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 4 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 5 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 6 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 7 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 9 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | A | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | b | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | c | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | d | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | E | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | F | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

1. Write the Boolean equation/expression for each of the output found in Table 1 (output a to g). Your solution must be in SOP (Sum of Products) form. Show all your work in deriving your solution by using Minterms. Label your inputs as D3, D2, D1, and D0. Label your outputs as a, b, c, d, e, f, and g.

Answer:

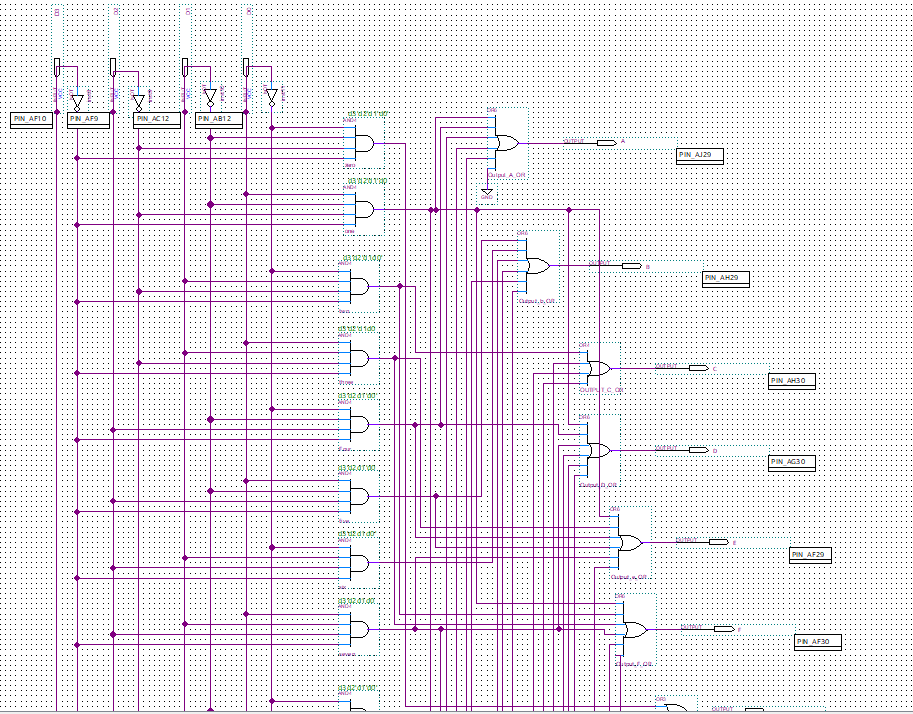
Inverted Expression:

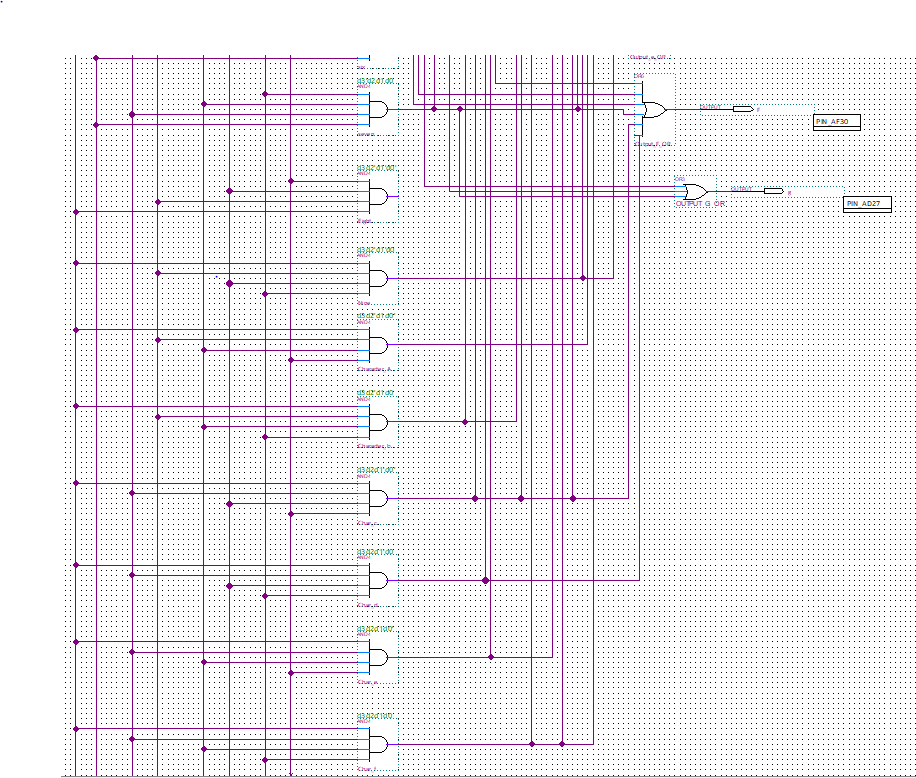
* A = D3’D2’D1’D0 + D3’D2D1’D0’ + D3D2’D1D0 + D3D2D1’D0’ + D3D2D1’D0
* B = D3’D2D1’D0 + D3’D2D1D0’ + D3D2’D1D0 + D3D2D1’D0’ + D3D2D1D0’ + D3D2D1D0
* C = D3’D2’D1D0’ + D3D2D1’D0’ + D3D2D1D0’ + D3D2D1D0
* D = D3’D2’D1’D0 + D3’D2D1’D0’ + D3’D2D1D0 + D3D2’D1’D0 + D3D2’D1D0’ + D3D2D1D0
* E = D3’D2’D1’D0 + D3’D2’D1D0 + D3’D2D1’D0’ + D3’D2D1’D0 + D3’D2D1D0 + D3D2’D1’D0
* F = D3’D2’D1’D0 + D3’D2D1D0 + D3D2D1’D0’ + D3lkoD2D1’D0
* G = D3’D2’D1’D0’ + D3’D2’D1’D0 + D3’D2D1D0

Normal Expression:

* A = D3’D2’D1’D0’+ D3’D2’D1’D0 + D3’D2’D1D0’+ D3’D2’D1D0 + (skip 4) + D3’D2D1’D0 + D3’D2D1D0’+ D3’D2D1D0+ D3D2’D1’D0’+ D3D2’D1’D0 + D3D2’D1D0’ + D3D2D1D0’+ D3D2D1D0
* B= D3’D2’D1’D0’+ D3’D2’D1’D0 + D3’D2’D1D0’+ D3’D2’D1D0 + D3’D2D1’D0’+ (skip 5,6) + D3’D2D1D0 + D3D2’D1’D0’+ D3D2’D1’D0 + D3D2’D1D0’+ D3D2D1’D0
* C= D3’D2’D1’D0’ + D3’D2’D1’D0 + D3’D2’D1D0+ D3’D2D1’D0’ + D3’D2D1’D0 + D3’D2D1D0’ + D3’D2D1D0+ D3D2’D1’D0’ + D3D2’D1’D0+ D3D2’D1D0’ + D3D2’D1D0 + D3D2D1’D0
* D= D3’D2’D1’D0’+(skip 1) + D3’D2’D1D0’+ D3’D2’D1D0 + (skip 4) D3’D2D1’D0 + D3’D2D1D0’+(skip 7) + D3D2’D1’D0’ (skip 9,A) + D3D2’D1D0+ D3D2D1’D0’+ D3D2D1’D0 + D3D2D1D0’
* E= D3’D2’D1’D0’+(skip 1) + D3’D2’D1D0’ + (skip 3,4,5) + D3’D2D1D0’+(skip 7) + D3D2’D1’D0’ (skip 9) + D3D2’D1D0’ + D3D2’D1D0 + D3D2D1’D0’+ D3D2D1’D0 + D3D2D1D0’ + D3D2D1D0
* F= D3’D2’D1’D0’ + (skip 1,2,3) + D3’D2D1’D'0’ + D3’D2D1’D0 + D3’D2D1D0’ + (skip 7) + D3D2’D1’D0’+ D3D2’D1’D0 + D3D2’D1D0’+ D3D2’D1D0 + (skip C,D) + D3D2D1D0’ + D3D2D1D0
* G= (skip 0,1) + D3’D2’D1D0’ + D3’D2’D1D0 + D3’D2D1’D0’ + D3’D2D1’D0 + D3’D2D1D0’ + (skip 7) + D3D2’D1’D0’ + D3D2’D1’D0 + D3D2’D1D0’ + D3D2’D1D0 + D3D2D1’D0’ + D3D2D1’D0 + D3D2D1D0’ + D3D2D1D0

Quartus Schematics:

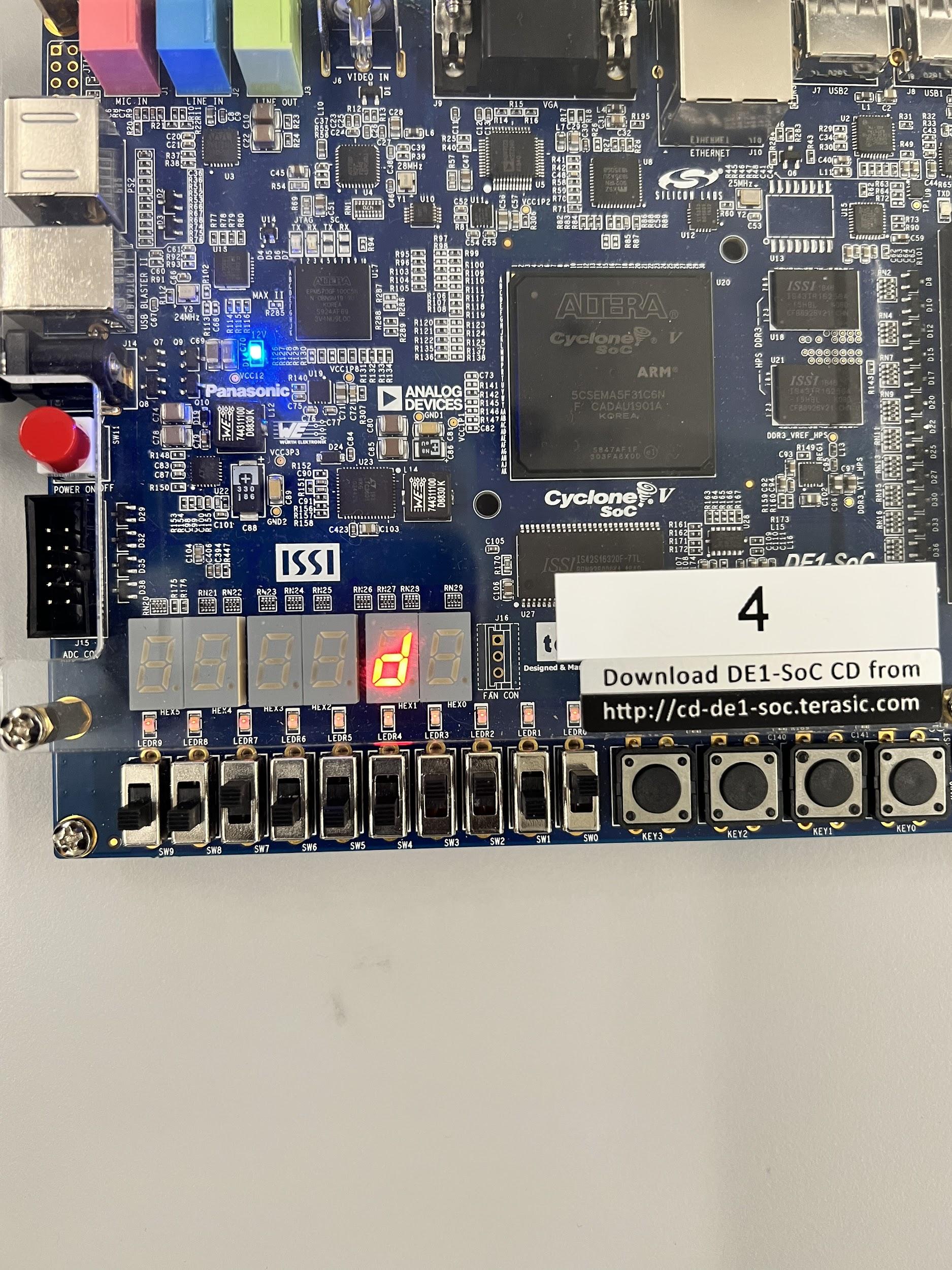


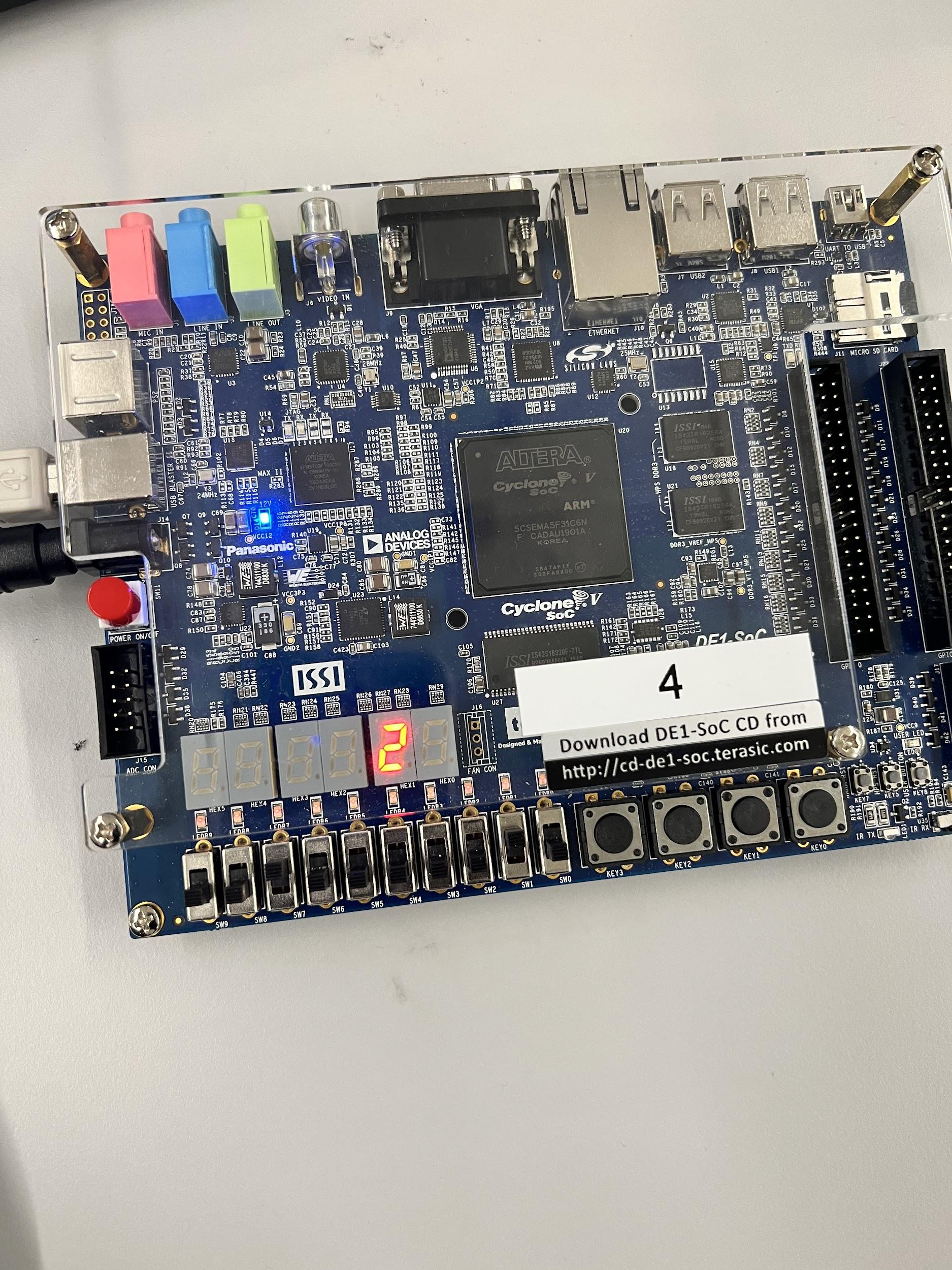
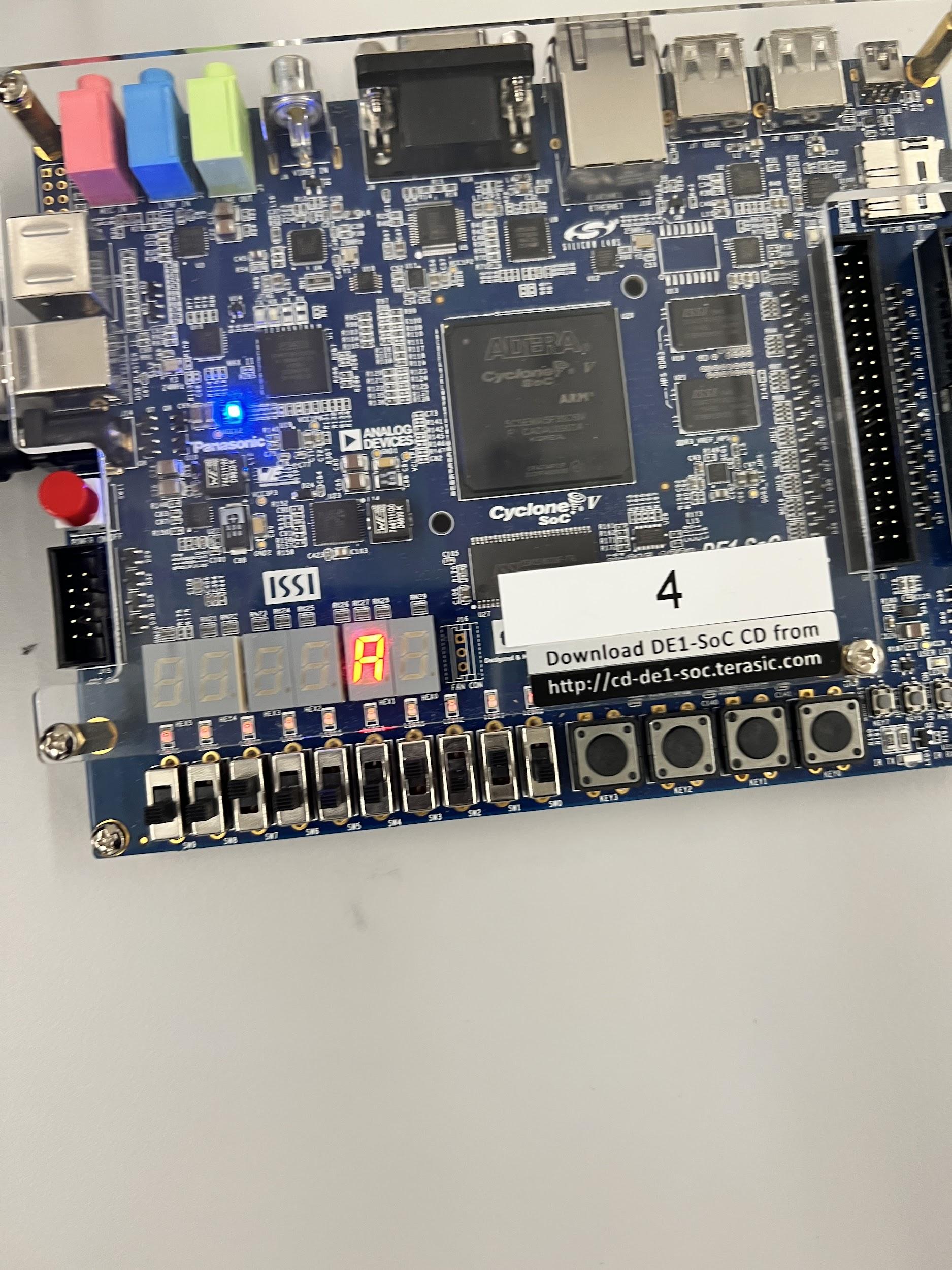


**1.1 Lab 1 Summary**

In this lab, the goal is to use AND, OR and NOT gates to implement the seven segment display on the DE1-SoC board. All segments on the 7-segment display are represented by different letters, which are controlled by 4 logic high/low inputs. By completing the table from prelab 1, the equations for all segments can be derived. Based off these equations, using SOP equation analysis, the schematic can be implemented on Quartus, which the times symbol can be put together as an AND gate and the plus symbol can be put together as an OR gate. However, the group used a different approach instead of normal SOP equation analysis. Since there are more 1s than 0s, inverting the table will be a better approach since it saves more work on finding the SOP equation and saves more space on the Quartus schematic.

The lab itself was self explanatory. The Quartus software was easy to use and Issues like incorrect pin assignments, and incomplete wiring diagrams were attributed to human error. We would recommend keeping your schematic in VLSI format as to mitigate any errors, and make it easier to spot your mistakes.

**Output Samples:**

****

# **References**

[1] Prof. Julius Marpaung, “*Lab Report Guide*”, Northeastern University, January 6 2020.

[2] Terasic, *DE1-Soc Manual, User Manual”,*January 28, 2019